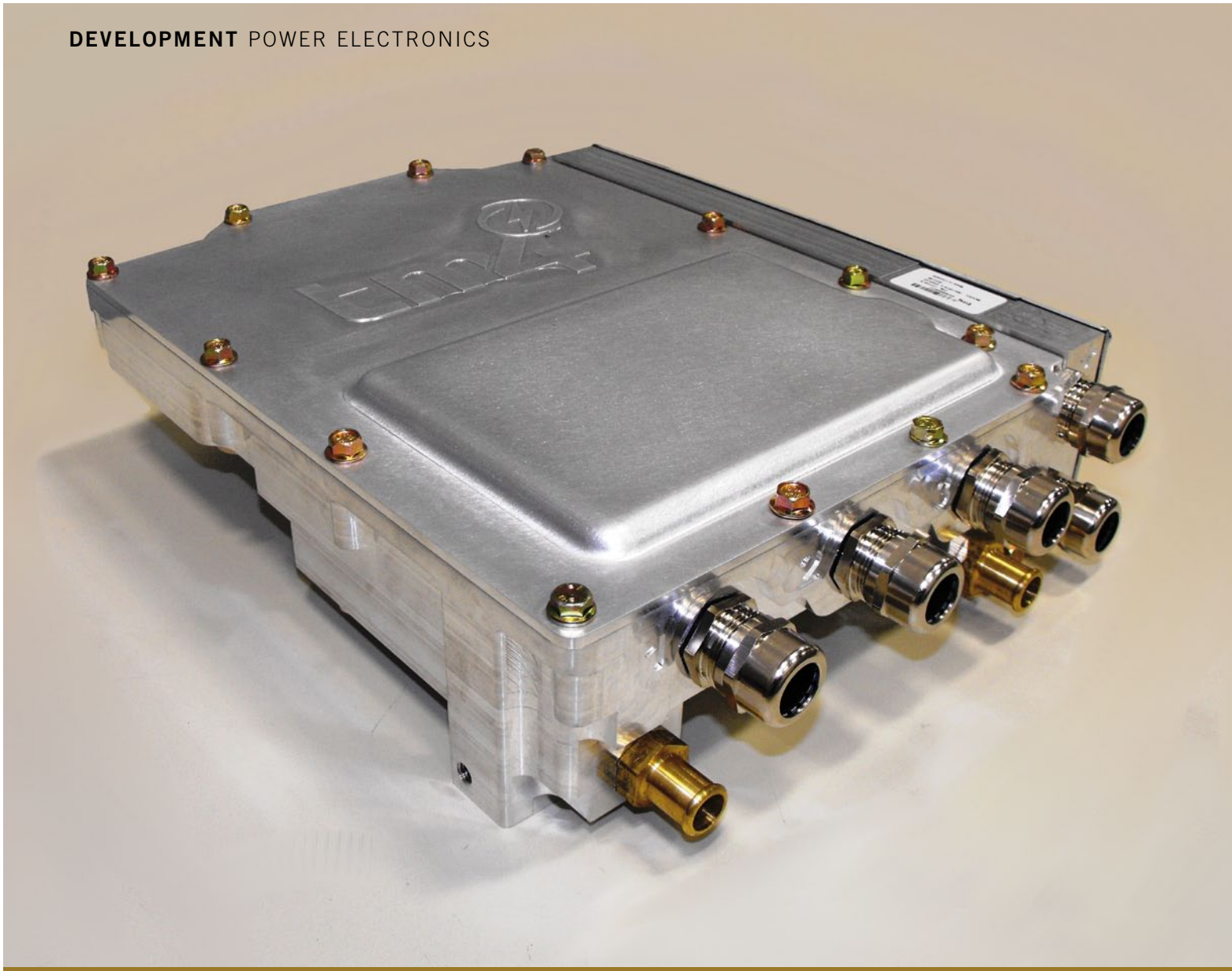

LIMITING THE OVERSHOOT ON IGBT DURING TURN-OFF USING STRAY INDUCTANCE

With the use of permanent magnet motors in the automotive drivetrain, the demand to finely control the current using power electronics has increased. Current is controlled by switching the IGBT On and Off at high frequencies. TM4 presents a new technique to control the overvoltage across the IGBTs of Electronic Motor Drive used in EV or HEV. The Canadian company demonstrates the major impact of overvoltage on the optimisation of the Power Train System as well as on efficiency.

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INITIAL SITUATION

The torque constant of the electric machine, e.g. like in Hybrid powertrains, has a direct impact on the maximum back EMF (E-motor counterforce) as well as the required phase current to provide a specific torque. It is therefore important to be able to operate at the highest possible bus voltage to allow a higher torque constant and lower phase current; to succeed, we must limit the overvoltage due to the parasitic inductance of the IGBT module to keep the peak voltage below the switches' maximum voltage rating.

The solution investigated at TM4, was to measure the voltage across the IGBTs and inject a gate current accordingly when the voltage exceeded a certain level. With this technique, life expectancy is barely impacted and reaction time can be compensated. Therefore, it remains difficult to protect against all operating conditions including different short circuits or overloads possible in the machine.

This research suggests using a part of the stray inductance of the IGBT module to sample the overvoltage; it slows down the gate voltage drop to limit the dI/dt during the turn-off process. Furthermore, it does not slow down the dV/dt thereby limiting the impact on efficiency. This article describes improvements made in TM4 and how we adapted it to IGBT module applications. A comparison with an Electronic Active Clamp will also be made.

PROBLEM STATEMENT

The equivalent circuit of a commutation cell is shown in ❶. When the IGBT is "On", the current circulates through V_{out}, L_{out}, Stray Inductance, IGBT and Cin. When the IGBT is Off, the current only circulates in V_{out}, L_{out} and the diode. The current change occurs in the loop incorporating the diode, the IGBT, the stray inductance and the input capacitor that is called High Frequency Loop. At turn-off, the voltage across the IGBT increases up to the bus voltage so the diode is positively polarised in order to start taking the current from the IGBT. A voltage is than generated by L_{stray}* dI/dt; this creates an overvoltage at the IGBT output.

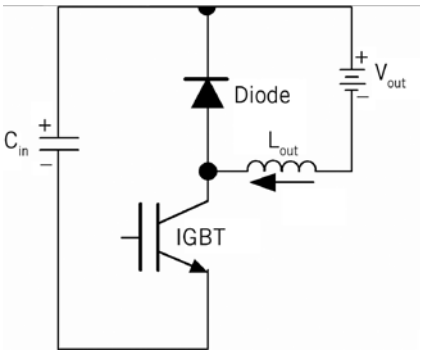
In order to reduce the overvoltage across the IGBT at turn-off, we need to reduce the stray inductance and/or the dI/dt in the high frequency loop. Choosing a capacitor with a parasitic inductance as low as possible and connecting it as close to the IGBT module as possible is all we can do to reduce the stray inductance of the high frequency loop. The following sections will address different possibilities to control the dI/dt.

IMPACTS ON EFFICIENCY WHEN LIMITING THE DI/DT

It is well known that limiting the dV/dt or dI/dt during the switching of a semiconductor will reduce efficiency. ❷ shows the two parts in the turn-off process: the voltage across Q1 increases up to the bus voltage (dV/dt). From zero to t1, the voltage across the IGBT increases up to the bus voltage and then a positive voltage is applied across D2. From t1 to t2, the current in the IGBT drops from load current to zero (dI/dt). By definition, the losses during turn-off are as follows:

EQ. 1	$E_{off} = \int_{toff} v(t)*i(t)*dt$

The losses depend on the product of the voltage and the current across the IGBT, and the time to turn it Off The tail current



❶ Equivalent circuit of a commutation cell

will add to the turn-off losses but is almost independent of the gate signal.

❸ shows the two parts of the turn-on process: the current increase in Q1 up to the load current plus the recovery current (dI/dt) during the first part to turn-off the diode D2 and the second part, is the drop of the voltage across Q1 (dV/dt). The difference between the IGBT voltage and the bus voltage is the voltage produced by L_{stray}*dI/dt during the first part (dI/dt). By definition, the losses during turn-on are as follows:

EQ. 2	$E_{on} = \int_{ton} v(t)*i(t)*dt$

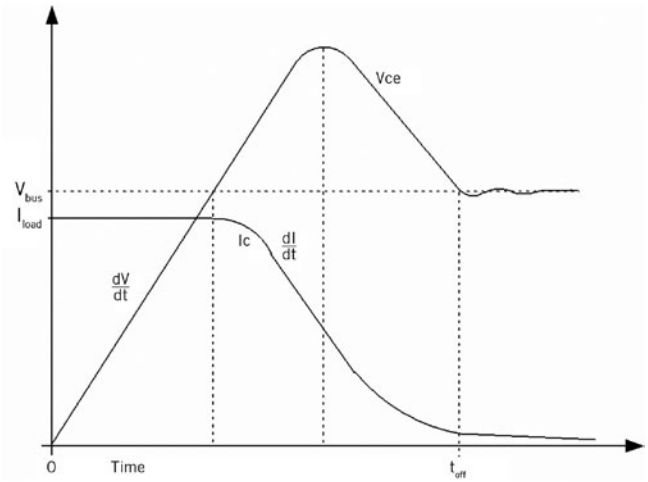
The positive effect of slowing down the dI/dt is that the turn-off of the opposite diode (D2) is very smooth so its losses are lower. The negative effect is the increase of the On-time.

USING THE STRAY INDUCTANCE TO LIMIT THE DI/DT

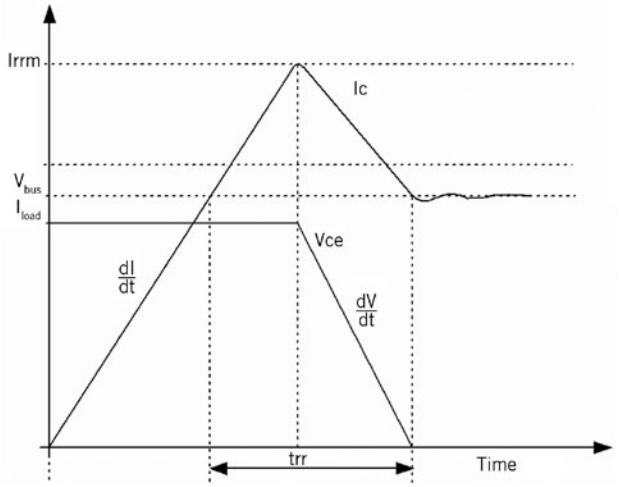
As demonstrated in the previous section, controlling the dI/dt at turn-off does limit the overvoltage across the IGBT; this section suggests that we limit the dI/dt using the stray inductance of the IGBT emitter. The idea is to inject a part of the total stray inductance voltage in the gate to slow its voltage drop during the turn-off process. The advantage of this technique is the direct action on the gate voltage without any delay and current limitations.

❹ shows the equivalent circuit of the IGBT leg with the gate drive circuit and the stray inductances of the module.

In order to include the emitter stray inductance into the gate drive, we connect



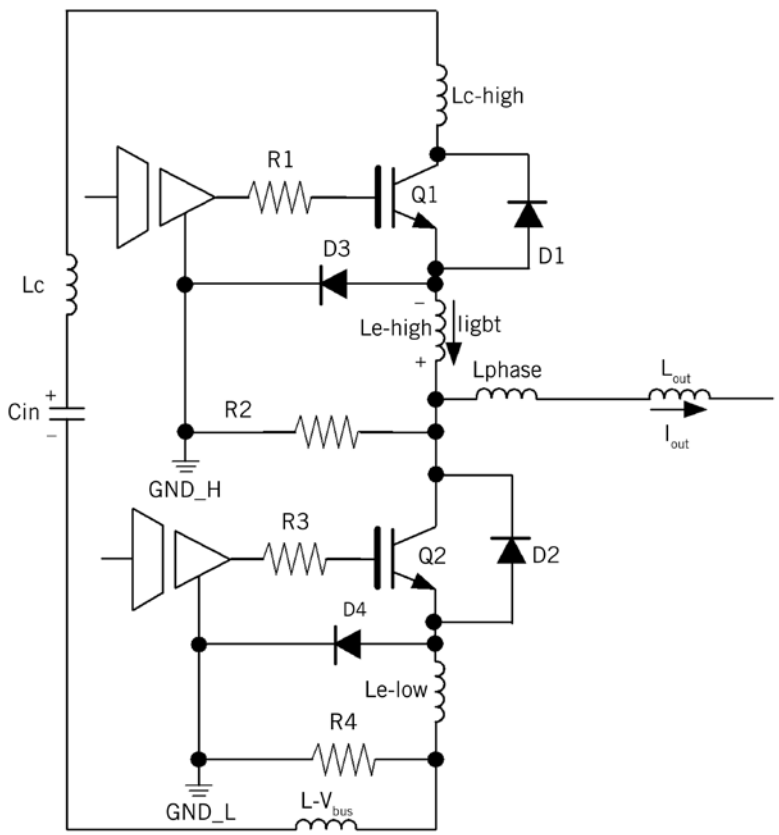
❷ Shape of the voltage and current across the IGBT at turn-off



❸ Shape of the voltage and current across the IGBTs at turn-on

the reference of the gate drive to a different physical location than the logical pins suggested by the manufacturer. In ② can be seen, that the overvoltage (above V_{bus}) increases with the same proportion as the slope of the current.

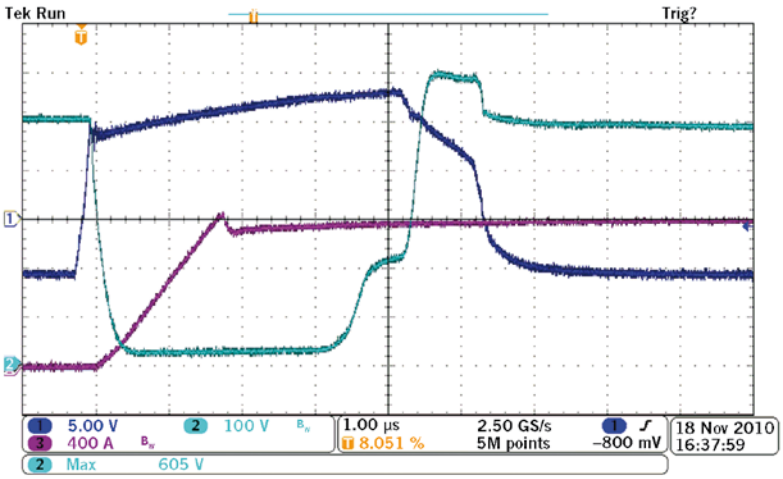
As an example, if Q1 is On and turns Off the current flowing in Le-high will decrease and create a voltage with the polarity indicated in ④. The emitter voltage will naturally decrease with the slope of the current relative to the gate drive reference connection. Therefore, it will limit the gate voltage drop. The voltage across Le-high is a sample of the voltage across the whole stray inductance of the high frequency loop that creates the overvoltage. This will slow down the commutation of the current from Q1 to D2 and increase the t_{off} and then the losses.



❹ Equivalent circuit of the IGBT module and the inductances of the connections

EXPERIMENTAL RESULTS

❺ shows an example of a turn-off of an IGBT under short-circuit conditions with a V_{bus} as high as 500 V. This test was performed on the lower IGBT. The overvoltage is very well controlled even if the current is almost four times the IGBT rating. This technique allows an IGBT rated at 600 V to operate at a voltage as high as 500 V, even in short-circuit conditions. We can also see the square shape of the overvoltage that optimises the lowest peak voltage and the lowest toff. This circuit was protected by a desaturation detection circuit; we can see the IGBT desaturation before opening. This example shows a spectacular result but in practice, we do not want to operate so near the IGBT maximum voltage rating because of the impact on efficiency. The dI/dt should be limited as much as the overvoltage. We can see the gate voltage (CH1) drop smoothly during the overvoltage and drop faster elsewhere. The current drop lasts for over 1 s which increases t_{off} Note that the current probe saturates at 1200 A and

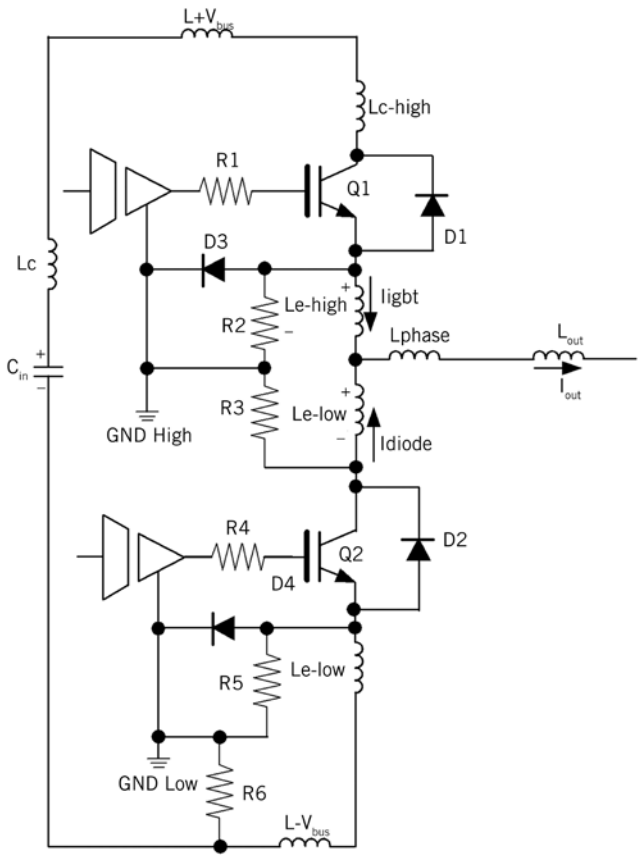


❺ Turn-off using the stray inductance to limit the overvoltage

keeps the same slope during the whole on-state.

Furthermore, because the upper emitter inductance is smaller by a large factor, it will not be possible to operate so near the IGBT maximum voltage rating with the upper IGBT.

The only current change during the first part of the commutation process (dV/dt up to the bus voltage) is the one that charges the output capacitors of the two IGBTs (Coes) that are very small; in conclusion, using the stray inductance to limit the dI/dt does not deteriorate the dV/dt.



❻ The resister divider is limiting the effect of the emitter inductance

OPTIMISATION OF THE EFFECT OF THE EMITTER INDUCTANCES

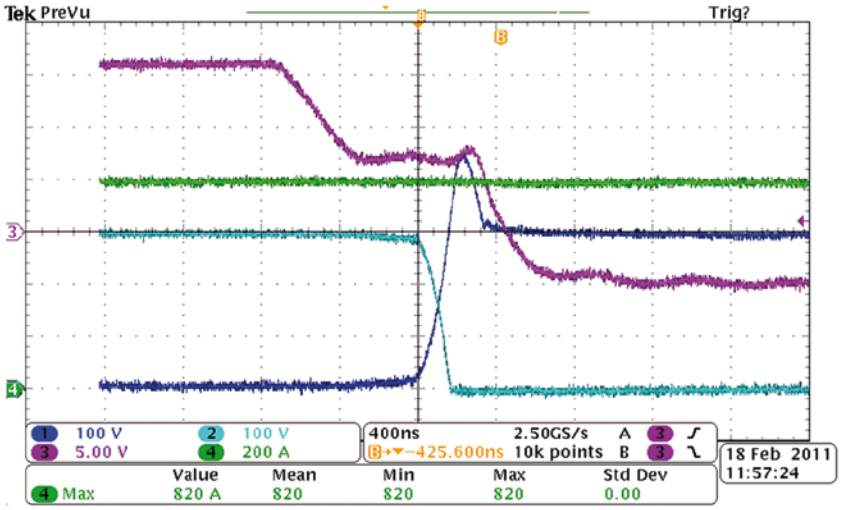
In the previous sections we saw that using the emitter inductances to slow down the dI/dt in the IGBTs has the effect of reducing the overvoltage; the higher the ratio of the emitter inductance over the total stray inductance, the lower the overvoltage will be but also the lower the efficiency will be. Because the modules come with their own stray inductance and emitter inductances and because the emitter inductances of the top and bottom IGBTs are not matched most of the time, it becomes difficult to find the compromise between an acceptable overvoltage and efficiency. This section proposes a way of reducing the effect of the emitter inductance to get the maximum overvoltage allowed to therefore get the best possible efficiency.

It is normal practice to use a resistor in the ground connection of the gate drive to limit the current in the diodes that protect the gate drive of the lower IGBT from a negative voltage when the upper IGBT turns off. We split this resistor in two and adapt the ratio between them to limit the effect of the emitter inductance on the dI/dt. R2 and R3, ❻, play that role for the upper IGBT and R5 and R6 for the lower IGBT. The total resistor remains the same but the voltage divider gives the desired weight of the emitter inductance.

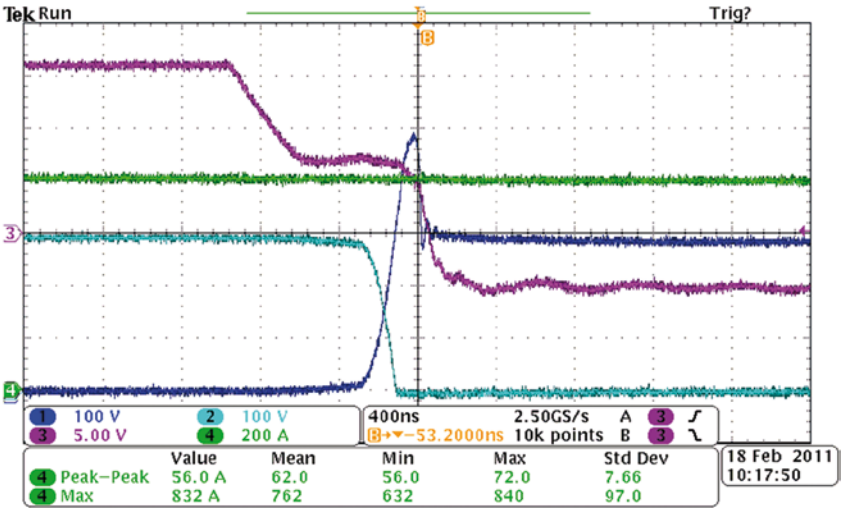
The overvoltage should obviously be optimised as much as possible to reach the maximum IGBT rating; this is done by reducing the resistor connected to the logical emitters compared to the resistor connected to the power tab. The voltage across the emitter inductance will be split in two and only the voltage across the logical resistor will be applied in the gate drive circuit to limit the gate voltage drop.

❼ shows the turn-off of an IGBT with the connection to the power tab, using the emitter inductance to limit the dI/dt and ❽ shows the same waveform in the same conditions using a resistive divider to optimise the overvoltage to get the best efficiency. We can see the overvoltage reaching 200 V with the resistive divider compared to only 150 without; it also reduces the duration of the overvoltage.

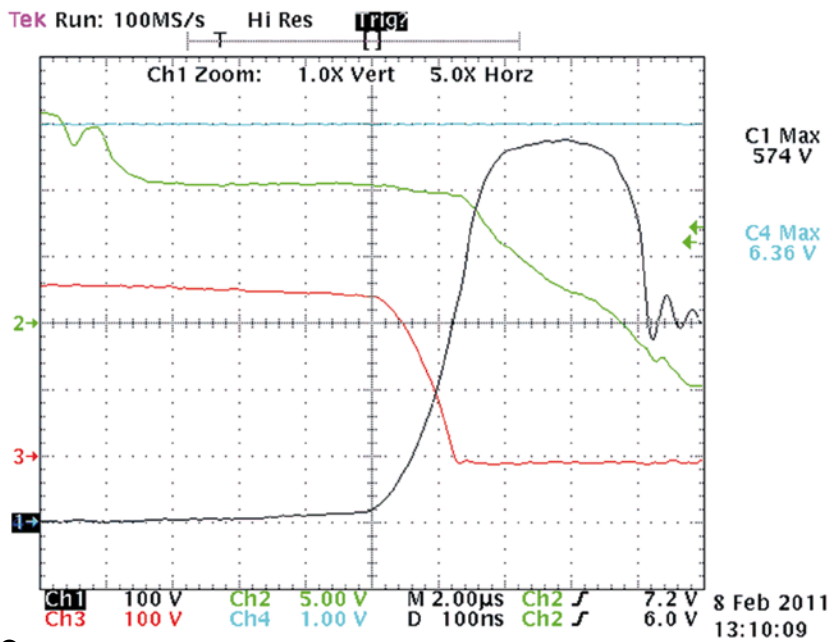
❾ shows a wave shape in short-circuit conditions with the same setup as ⑧. We can see the square shape of the voltage



❼ Turn-off without optimisation of the emitter inductance



❽ Turn-off with optimisation of the emitter inductance



❾ Turn-off in short-circuit condition with a bus voltage of 350 V

that almost goes up to the 600 V IGBT rating. As explained above, the square shape represents the best compromise between the peak voltage and the dI/dt duration.

CONCLUSION

After a review of the major root causes of the overvoltage problem across the IGBTs in Power Electronic Drive Motors, TM4 made a review of the potential solutions.

We compared the new technique with the Electronic Active Clamp developed at TM4 and presented the differences supported by experimental results.

The new technique is based on the use of the parasitic inductance of the IGBTs module, the root cause of the overvoltage, which is normally undesirable, to slow down the dI/dt. We have also developed a way to optimise the use of the Stray Inductance in order to become independent of the packaging of the IGBT module. Experimental results demonstrated how powerful the new technique is, using the Stray Inductance, in any load conditions including overload and short-circuit.

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